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10/693,546	10/23/2003	John R. Chase	ALTRP098/A1185	3624

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BEYER WEAVER LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,546	CHASE, JOHN R.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been presented for examination.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 25-27 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, claims 25-27 are directed to software per se as the broadest reasonable interpretation for the means for the claimed apparatus includes software means only (page 19 of the Specification, last paragraph). Furthermore, the invocation of U.S.C. 112, 6th paragraph is invalidated due to lines 15-19 on page 19 of the Specification of the instant application as all possible means for embodiment are disclosed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-13 and 17-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1) in view of Heinkel et al. (U.S. Patent Application Publication 2004/0015739 A1).**

As per claim 1, Zaidi is directed to a method **([0029]-[0032])** comprising: a plurality of test designs **([0037])**, the plurality of test designs having varied characteristics **([0054])** to allow testing of a design automation tool, wherein generating one of the plurality of test designs comprises: instantiating the I/O structure of a top level module, the top level module having input and output pins **([0048]-[0052])**; *selecting a plurality of submodules* **([0074])** *from a design module library* **([0055])**, *wherein cost constraints are used to select the plurality of submodules* **([0076]-[0078])**; parameterizing *the* plurality of submodules from *the* design module library for interconnection with the top level module, the plurality of submodules having input and output lines **([0039, Table 1])**; providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module **([0050])** but fails to explicitly disclose generating a plurality of test designs.

Heinkel teaches generating a plurality of test designs **([0057]-[0060]).** Specifically, Heinkel **[0057])** teaches it is possible to "reconfigure the device under test" which anticipates generating multiple test designs and applying the plurality of test designs to test the design automation tool **([0058])**. Zaidi and Heinkel are analogous art because they are from the same field of endeavor, validating an IC with a testbench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of validating an IC of Zaidi with the method of generating test designs of Heinkel in order to allow testing of different

designs without needing to recompile the VHDL testbench for each test design **(Heinkel, [0058])**.

As per claim 2, the combination of Zaidi and Heinkel already discloses the method of claim 1, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip **(Zaidi, [0031])**.

As per claim 3, the combination of Zaidi and Heinkel already discloses the method of claim 1, wherein the design automation tool is used to implement designs on an ASIC **(Zaidi, [0029])**.

As per claim 4, the combination of Zaidi and Heinkel already discloses the method of claim 1, wherein *instantiation constraints are used to select the plurality of submodules* **(Zaidi, [0085])**.

As per claim 5, the combination of Zaidi and Heinkel already discloses the method of claim 1, wherein the design automation tool is a synthesis or a place and route tool **(Zaidi, [0032])**.

As per claim 6, the combination of Zaidi and Heinkel already discloses the method of claim 1, wherein providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs **(Zaidi, [0048]-[0060])**.

As per claim 7, the combination of Zaidi and Heinkel already discloses the method of claim 6, wherein inputs comprise input pins of the top level module, submodule output lines, and registers **(Zaidi, [0048]-[0060])**.

As per claim 8, the combination of Zaidi and Heinkel already discloses the method of claim 6, wherein outputs comprise output pins of the top level module, submodule input lines, and registers **(Zaidi, [0048]-[0060])**.

As per claim 9, the combination of Zaidi and Heinkel already discloses the method of claim 8, wherein providing logic to interconnect the plurality of parameterzied modules but does not disclose classifying inputs and outputs as clock lines, control lines, and data lines. Official notice is taken with respect to this limitation. Specifically it would have been obvious to one of ordinary skill in the art at the

time of Applicants invention to have this feature in order to prevent errors when interconnecting inputs and outputs.

As per claim 10, the combination of Zaidi and Heinkel already discloses the method of claim 8, wherein generating one of the plurality of test designs further comprises: *generating randomized logic* **(Zaidi, [0048]-[0060])**

As per claim 11, the combination of Zaidi and Heinkel already discloses the method of claim 10, randomized *is generated* logic to drive outputs **(Zaidi, [0047])**.

As per claim 12, the combination of Zaidi and Heinkel already discloses the method of claim 10, wherein generating randomized logic comprises directly wiring outputs to inputs, generating a logic expression using inputs, generating a mathematical expression using inputs, or generating decision logic **(Zaidi, [0047])**.

As per claim 13, the combination of Zaidi and Heinkel already discloses the method of claim 6, but fails to disclose wherein parameterizing the plurality of submodules comprises defining interfaces, data width, and the type of signal for input and output lines associated with the submodule. Official notice is taken with respect to this limitation. Specifically it would have been obvious to one of ordinary skill in the art at the time of Applicants invention to have this feature in order to prevent errors when interconnecting inputs and outputs.

As per claim 15, the combination of Zaidi and Heinkel already discloses the method of claim 6, wherein generating one of the plurality of test design further comprises selecting a clock structure for each output **(Zaidi, [0047])**.

As per claims 17-24, Zaidi discloses a computer system **([0029]-[0032])**, comprising: memory operable to hold information associated with a design module library **([0025])**, a processor coupled to memory **([0025])**, the processor configured to execute a method with the same limitations of claim 1 and is therefore rejected over the same art combination.

As per claim 25-27, Zaidi is directed to an apparatus for generating test a testbench **([0029]-[0032])**, the apparatus comprising: means for a method with the limitations of claim 1 and is therefore rejected over the same art combination.

4. **Claims 14 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1) and Heinkel et al. (U.S. Patent Application Publication 2004/0015739 A1) **in further view of Goossens ("Design of Heterogeneous ICs for Mobile and Personal Communication Systems").**

As per claim 14, the combination of Zaidi and Heinkel is directed to the method of claim 6, wherein submodules comprise memory and timers **([0037])** but fails to disclose wherein submodules comprise adders and phase lock loops. Goossens teaches submodules comprising of adders and phase lock loops **(page 524-525, Figure 1, Section 3.2)**. Zaidi, Heinkel, and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of validating an IC with a testbench of Zaidi and Heinkel with the adders and phase lock loops of Goossens in order to allow the design of heterogeneous IC architecture **(page 524, Section 1)**.

As per claim 16, the combination of Zaidi and Heinkel is directed to the method of claim 15, but fails to specifically disclose wherein clock structures include a plurality of synchronous and asynchronous structures. Goossens teaches clock structures that include a plurality of synchronous and asynchronous structures **(page 525-526, Section 3.3)**. Zaidi, Heinkel, and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of validating an IC with a testbench of Zaidi and Heinkel with the clock structures of Goossens in order to implement handshaking, protocol control, and synchronization functionalities for heterogeneous IC architecture **(page 525-526, Section 3.3)**.

Response to Arguments

5. Applicant's arguments filed 03/05/07 have been fully considered but they are not persuasive.

6. 35 U.S.C. 101 rejections of claims 1-24 are withdrawn. Rejection of claims 25-27 are maintained as they are still directed to software per se which is nonstatutory.

7. In response to Applicant's argument that Zaidi and Heinkel do not teach or suggest "selecting a plurality of submodules from a design module library, wherein cost constraints are used to select the plurality of submodules", Applicant is further directed to Zaidi as it anticipates selecting a plurality of submodules **[0074]** for synthesis of a test design from a design module library **[0055]** wherein cost constraints are used for synthesis of a test design **[0076]-[0078]**. Furthermore, Zaidi anticipates using instantiation constraints to select the plurality of submodules **[0085]**.

8. In response to Applicant's argument that the limitation of generating multiple test designs is not anticipated by Zaidi or Heinkel, as noted in previous Office Actions, Applicant is further directed to Zaidi, paragraphs **[0040]-[0041]**. As the "<block>/sim/" directory includes simulation test for the design in **[0037]**, the "<newblock>/sim/" directory includes simulation test for different test designs where new blocks are added onto the design and additional tests for the system with new blocks can be executed from said directory. Additionally, Applicant is directed to Zaidi, paragraph **[0054]** where users may configure particular blocks or systems in multiple ways for a top level testbench. As noted in previous Office Actions, the Applicant is also further directed to Heinkel, paragraph **[0057]** where it is possible to "reconfigure the device under test" and thus anticipates generating multiple test designs. Heinkel does so as the device under test is reconfigurable; as known by an ordinary person skilled in the art when the device is first configured with one test design but later reconfigured with a different test design, while only one physical device exists, a plurality of test designs have been generated.

9. Applicant appears to allege that Zaidi tests physical blocks which does not anticipate the test design of the present invention includes a processor and DSP core. Zaidi teaches the

10. While Applicant states "Both Heinkel and Zaidi possibly describe scripts and simulations that are used to test a physical block or a "new block" " that does not prohibit the scripts and simulations of Heinkel and Zaidi to allow testing of a design automation tool.

Conclusion

11. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 6,477,691 B1 issued to Bergamashi/Rab et al. on 11/05/02.

2. U.S. Patent Application Publication No. 2004/0015792 A1 published by Kubista on 01/22/04.

3. U.S. Patent No. 6,053,947 issued to Parson on 04/25/00.

4. "ASIC to FPGA Design Methodology & Guidelines" published by Altera in July 2003.

5. U.S. Patent No. 7,085,702 issued to Hwang et al. on 08/01/06.

6. U.S. Patent Application Publication No. 2004/0210798 A1.

12. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
05/11/07

KAMINI SHAH
SUPERVISORY PATENT EXAMINER